SEMI-CONDUCTORS

INTERFACES

Investigation on silicon wafers for improved manufacturing process of integrated circuits

The fabrication of integrated circuits often involves multilayer structures stacking different materials – metals and dielectrics - on a silicon substrate.

THE PROBLEM TO SOLVE:

Delamination (i.e. separation of layers) may occur at some point during the process and causes severe equipment downtime. The semiconductor industry would like to prevent this risk.

A STEP TOWARDS THE SOLUTION

Wafers exhibiting delamination (Figure 1) have been investigated using neutron reflectometry. An intermediate layer has been found which is mainly composed of Hydrogen between other known layers (Figure 2).

Characteristics (e.g. thickness, roughness) of the intermediate layer for both delaminated and non-delaminated wafers have been derived from measurements and several parameters are pointed out as responsible for the lack of adhesion between layers.

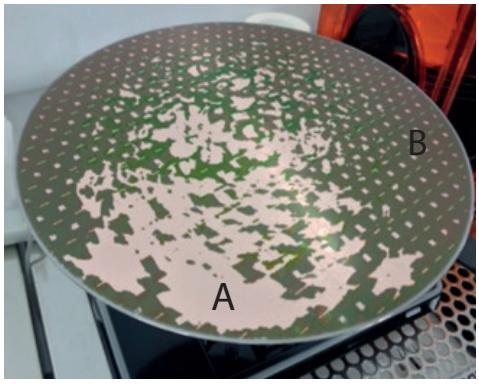

Fig. 1 A 300 mm wafer exhibiting delamination areas.

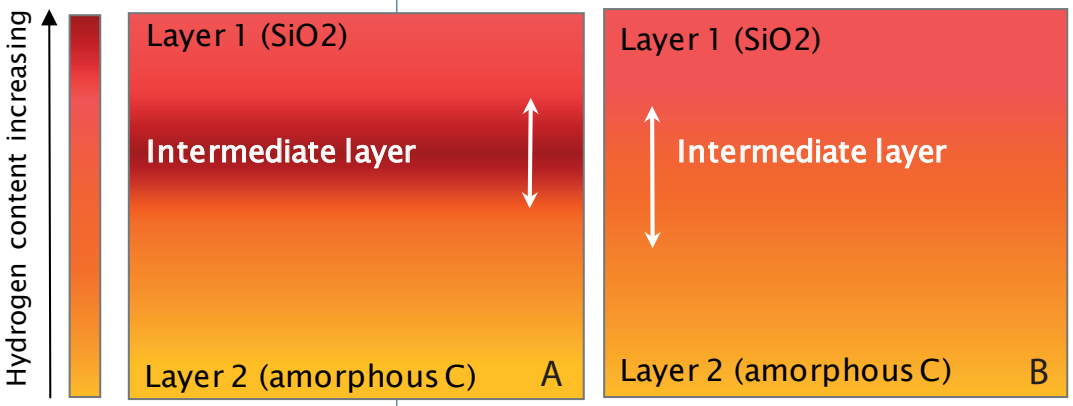

Fig. 2 Schematic view of hydrogen content within the layers investigated. A is where there are delamination sites and B is where there are no delamination sites. The wafer that undergoes delamination (A) has a high content of H within the intermediate layer.

THE RESULT

The characterization of the layers has led to the identification of the parameters to be controlled during the manufacturing process.

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http://sine2020.eu/industry.html

Reference: J Segura-Ruiz, P. Gutfreund, G. Imbert, A. Ponard, R. Cubitt, J Appl Phy, 215302 (2015)

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